Amendments of the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the above-identified patent application.

Listing of Claims

1. (currently amended) A programmable logic device comprising:

a plurality of logic elements (LEs) for performing logic functions that are arranged in one or more logic array blocks (LABs);

at least one input/output (I/O) block for passing signals between said LEs and one or more I/O pads associated with said I/O block, said I/O pads providing input and output to said programmable logic device; and

a signal routing architecture for routing signals among said LEs and said at least one I/O block comprising:

a plurality of horizontal and vertical signal routing conductors and drive circuitry;

at least one block input multiplexer for selectively providing signals from said plurality of horizontal and vertical signal routing conductors to said at least one I/O block; and

at least one output bypass path for providing a direct connection between an output from one of said plurality of LEs and said at least one I/O block, wherein said at least one output bypass path does not travel through a multiplexer between said plurality of LEs and said at least one I/O block.

2. (original) The programmable logic device of claim 1 wherein said at least one output bypass path is used for routing a data signal.

3. (original) The programmable logic device of claim 1 wherein said at least one output bypass path is used for routing an output enable signal.

4. (original) The programmable logic device of claim 1 wherein said at least one output bypass path is used for routing signals to an I/O register.

5. (original) The programmable logic device of claim 1 wherein said at least one output bypass path is used for routing signals to an external phase-locked loop circuit.

6. (original) The programmable logic device of claim 1 wherein said at least one output bypass path is used for routing signals to a memory controller.

7. (original) The programmable logic device of claim 1 wherein said at least one I/O block comprises at least one I/O multiplexer, said output bypass path being coupled to one of the inputs of said at least one I/O multiplexer.

8. (original) The programmable logic device of claim 7 wherein said at least one I/O block further comprises at least one output buffer, the output of said at least one I/O multiplexer being coupled through said output buffer to one of said I/O pads.

9. (original) The programmable logic device of claim 7 wherein said at least one I/O block further comprises one or more I/O registers.

10. (original) The programmable logic device of claim 7 wherein said at least one I/O block further comprises one or more output enable multiplexers.

11. (original) The programmable logic device of claim 1 wherein said at least one I/O block comprises:

an I/O multiplexer;

a bypass multiplexer receiving as one of its inputs the output of said I/O multiplexer, wherein said output bypass path is coupled to another of the inputs of said bypass multiplexer; and

an output buffer, wherein the output of said bypass multiplexer is coupled through said output buffer to one of said I/O pads.

12. (original) The programmable logic device of claim 1 wherein said LABs are arranged in a one dimensional array.

13. (original) The programmable logic device of claim 1 wherein said LABs are arranged in a two dimensional array.

14. (original) The programmable logic device of claim 1 wherein said drive circuitry comprises a driver input multiplexer (DIM) and a driver.

15. (original) The programmable logic device of claim 1 wherein said drive circuitry comprises a buffer and one or more programmable switches.

16. (original) The programmable logic device of claim 15 wherein said one or more programmable switches are pass transistors.

17. (original) The programmable logic device of claim 1 wherein said drive circuitry comprises:

a multiplexer;

a driver; and

one more programmable switches.

18. (original) A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 1 coupled to the processing circuitry and the memory.

19. (original) A printed circuit board on which is mounted a programmable logic device as defined in claim 1.

20. (original) The printed circuit board defined in claim 19 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

21. (original) The printed circuit board defined in claim 20 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

22. (original) An integrated circuit device comprising the programmable logic device of claim 1.

23. (original) A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

an integrated circuit device as defined in claim 22 coupled to the processing circuitry and the memory.

24. (original) A printed circuit board on which is mounted an integrated circuit device as defined in claim 22.

25. (original) The printed circuit board defined in claim 24 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the integrated circuit device.

26. (original) The printed circuit board defined in claim 25 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

27. (currently amended) A programmable logic device comprising:

a plurality of programmable logic circuits;

an I/O circuit;

programmable interconnection circuitry for selectively conveying signals between the logic circuits;

programmable routing circuitry for programmably selecting from any of a plurality of signals in the interconnection circuitry a signal for application to the I/O circuit; and

programmable bypass circuitry for selectively conveying a signal from one of the logic circuits to the I/O circuit in lieu of a signal from the routing circuitry <u>without traveling through programmable routing circuitry between said plurality of LEs and said at least one I/O block</u>.

28. (original) A programmable logic device comprising:

a plurality of logic elements (LEs) for performing logic functions that are arranged in one or more logic array blocks (LABs);

at least one input/output (I/O) block for passing signals between said LEs and one or more I/O pads, said I/O pads providing input and output to said PLD; and

a signal routing architecture for routing signals among said LEs and said at least one I/O block comprising:

a plurality of segmented routing conductors and drive circuitry;

at least one driver input multiplexer for selectively providing signals from said at least one I/O block to one or more of said plurality of segmented routing conductors; and

at least one input bypass path for providing a direct connection between said at least one I/O block and one of said plurality of segmented routing conductors dangling at the boundary of said routing architecture.

29. (original) The programmable logic device of claim 28 wherein said at least one I/O block comprises an input buffer, said input bypass path providing a direct connection between said input buffer and said one of said plurality of segmented routing conductors.

30. (currently amended) A method of increasing the speed of a programmable logic device comprising:

configuring a plurality of logic elements (LEs) for performing logic functions in one or more logic array blocks (LABs); and

using a signal routing architecture that comprises at least one block input multiplexer for routing signals among said LEs and at least one I/O block, said signal routing architecture providing at least one direct connection between an output from one of said LEs and said at least one I/O block, wherein said at least one direct connection does not travel through a multiplexer between said LEs and said at least one I/O block.

31. (original) A method of increasing the speed of a programmable logic device comprising:

configuring a plurality of logic elements (LEs) for performing logic functions in one or more logic array blocks (LABs);

using a signal routing architecture that comprises a plurality of segmented routing conductors for routing signals among said LEs and at least one I/O block,

said signal routing architecture comprising at least one driver input multiplexer for selectively providing signals from said at least one I/O block to at least one of said plurality of segmented routing conductors; and

providing at least one direct connection between said at least one I/O block and one of said plurality of segmented routing conductors dangling at the boundary of said routing architecture.